

CLAIMS

What is claimed is:

- 1        1.     A method of memory management, comprising :  
2        providing multiple banks of memory devices organized into  
3        independent channels wherein each bank of memory devices contains  
4        duplicate data;  
5        providing a tree memory controller for controlling data read and write  
6        accesses to each of the banks in each of the channels;  
7        establishing a bank queue for each bank in each channel for  
8        designating bank availability;  
9        sending read or write requests to the tree memory controller;  
10        checking, at the tree memory controller, the availability of each bank in  
11        a channel;  
12        identifying a first available bank; and  
13        executing the read request from the first available bank.
  
- 1        2.     The method of claim 1 wherein the step of executing for a write  
2        access includes:  
3        blocking all read requests;  
4        confirming that data to be written is complete for the selected memory  
5        word length;  
6        waiting for each bank queue to indicate bank availability for all banks;  
7        initiating burst mode transfer of the completed data word to all banks  
8        concurrently.
  
- 1        3.     The method of claim 1 wherein the memory devices comprise  
2        dynamic random access memory (DRAM) devices.
  
- 1        4.     The method of claim 1 wherein the memory devices comprise  
2        fast cycle random access memory (FCRAM) devices.
  
- 1        5.     The method of claim 1 wherein the banks of memory devices

2 are organized into two independent channels.

1       6.    A method system, comprising:  
2        multiple banks of memory devices organized into independent  
3        channels wherein each bank of memory devices contains duplicate data;  
4        a tree memory controller for controlling data read and write accesses to  
5        each of the banks in each of the channels;  
6        a bank queue for each bank in each channel for designating bank  
7        availability; and  
8        means for sending read or write requests to the tree memory controller,  
9        said controller determining availability of a bank for reading data and  
10      executing the read request from a first available bank.

1       7.    The system of claim 6 wherein the controller suspends all read  
2        requests during processing of a write request.

1       8.    The system of claim 7 wherein the controller writes to all  
2        memory banks concurrently.

1       9.    The system of claim 8 wherein all memory banks contain  
2        identical data.

1       10.   The system of claim 6 wherein the memory banks comprise  
2        dynamic random access memory devices.

1       11.   The system of claim 6 wherein the memory banks comprise fast  
2        cycle random access memory devices.

1       12.   The system of claim 6 wherein the banks of memory devices are  
2        arranged in two independent channels.

13.    The system of claim 6 wherein the minimum number of memory  
      banks is determined by the ratio of the random cycle time to the random bank  
      access delay.